

# Exhibit 6

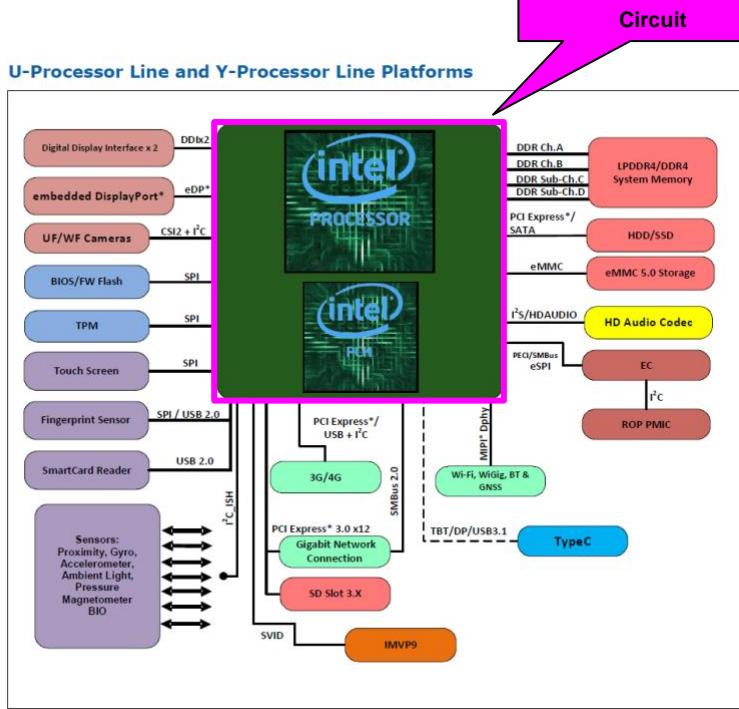
## U.S. Patent No. 8,193,792 (“’792 Patent”)

### **Accused Products**

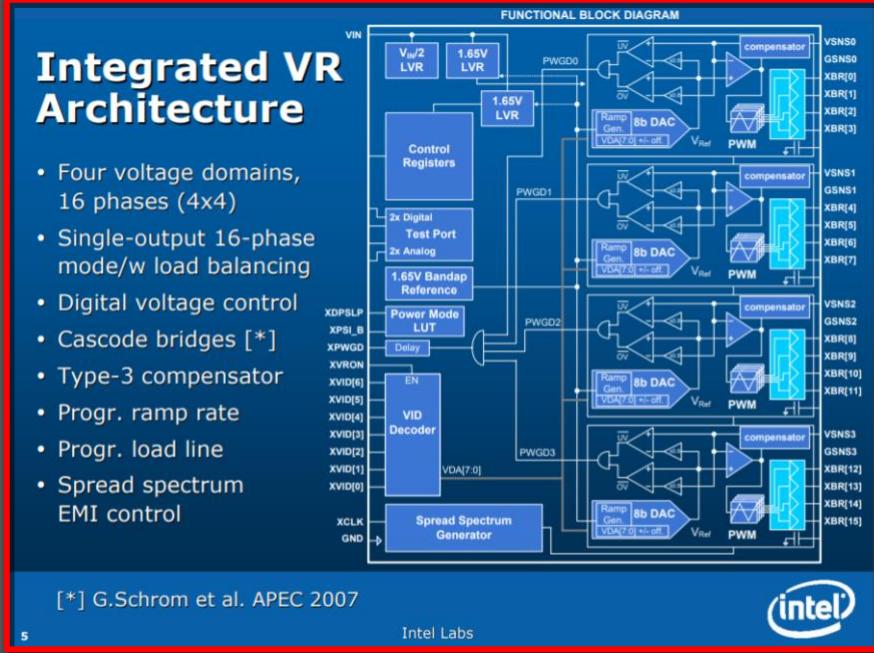
Dell products with Intel processors featuring Fully Integrated Voltage Regulators, including without limitation the Dell XPS 13 7390 (“Accused Products”), infringe at least Claims 1 and 10 of the ’792 Patent.

### **Claim 1**

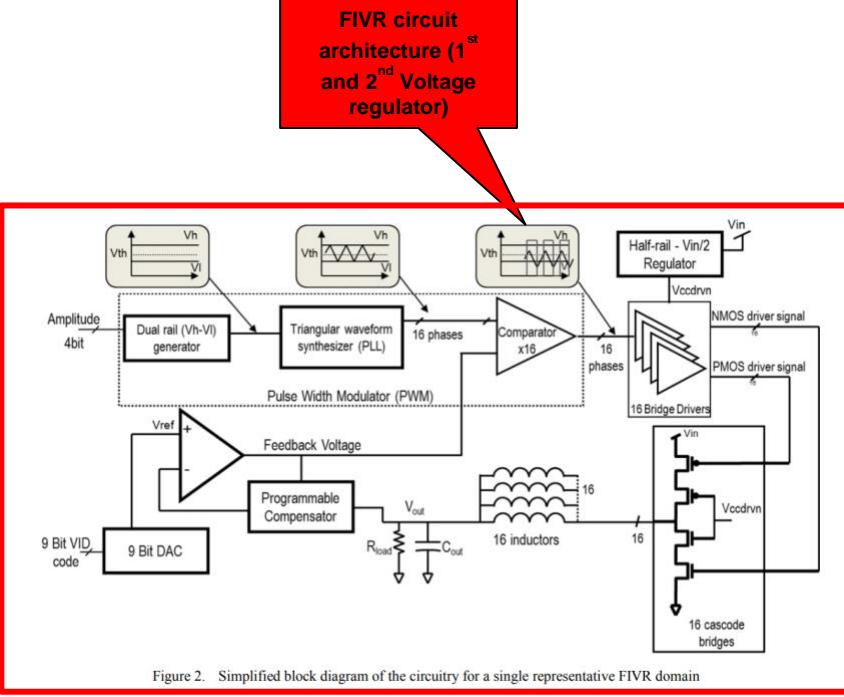
Claim 1	Accused Products
[1pre] A circuit comprising:	<p>To the extent the preamble is limiting, each Accused Product comprises the claimed circuit.</p> <p>For example, the XPS 13 7390 includes a 10th-generation Intel Core processor, which contains Intel Fully Integrated Voltage Regulator technology.</p> <p><i>See, e.g.:</i></p> <p><b>The most powerful 13-inch laptop in its class*</b>: With up to new 10th Gen Intel® Quad Core processors, more cores means increased performance, even with multiple applications running. Plus, Dell Power Manager, engineered by Dell, allows users to customize their laptop acoustics (fan speeds), temperature and performance based on their preferences between quiet, ultra-performance and cool modes. For example, quiet mode is 50% quieter than the other modes. It also dynamically delivers the maximum power from your processor while monitoring and managing system temperatures. When you see the “Engineered for mobile performance” icon next to select Dell PCs, you know it was designed to keep up with your fast-paced life.</p> <p>Screenshot from <a href="https://www.dell.com/en-us/shop/dell-laptops/xps-13-7390-laptop/spd/xps-13-7390-laptop">https://www.dell.com/en-us/shop/dell-laptops/xps-13-7390-laptop/spd/xps-13-7390-laptop</a></p>

Claim 1	Accused Products
	<p style="text-align: center;"><b>Figure 1-1. U-Processor Line and Y-Processor Line Platforms</b></p>  <p>The diagram illustrates the internal architecture of Intel U-Processor and Y-Processor platforms. At the center is the Intel Processor, connected to various components via internal buses. External connections include:</p> <ul style="list-style-type: none"> <li>Digital Display Interface x 2 (DDI2)</li> <li>embedded DisplayPort* (eDP*)</li> <li>UF/WF Cameras (CSI2 + I<sup>2</sup>C)</li> <li>BIOS/FW Flash (SPI)</li> <li>TPM (SPI)</li> <li>Touch Screen (SPI)</li> <li>Fingerprint Sensor (SPI / USB 2.0)</li> <li>SmartCard Reader (USB 2.0)</li> <li>Sensors: Proximity, Gyro, Accelerometer, Ambient Light, Pressure, Magnetometer, BIO (I<sup>2</sup>C ISH)</li> <li>PCI Express*/USB + I<sup>2</sup>C (3G/4G, Gigabit Network Connection, SD Slot 3.X)</li> <li>PCI Express* 3.0 x12 (SMBus 2.0)</li> <li>Wi-Fi, WiGig, BT &amp; GNSS (I<sup>2</sup>S - DAI)</li> <li>TBT/DP/USB3.1 (TypeC)</li> <li>IMVP9 (SVID)</li> <li>LPDDR4/DDR4 System Memory (DDR Ch.A, DDR Ch.B, DDR Sub-Ch.C, DDR Sub-Ch.D)</li> <li>HDD/SSD (PCI Express*/SATA)</li> <li>eMMC (eMMC 5.0 Storage)</li> <li>HD Audio Codec (I<sup>2</sup>S/HDAUDIO)</li> <li>EC (PCI/IMMbus eSPI)</li> <li>ROP PMIC (I<sup>2</sup>C)</li> </ul> <p>A pink arrow points from the word "Circuit" in the header to the central Intel Processor component.</p> <p>Screenshot, with annotation illustrating the claimed circuit, from <a href="https://www.intel.com/content/www/us/en/products/docs/processors/core/10th-gen-core-families-datasheet-vol-1.html">https://www.intel.com/content/www/us/en/products/docs/processors/core/10th-gen-core-families-datasheet-vol-1.html</a></p>
[1a] a first voltage regulator;	<p>Each Accused Product includes a first voltage regulator.</p> <p>For example, the XPS 13 7390 includes an Intel 10th-generation Core processor featuring Intel's Fully Integrated Voltage Regulator ("FIVR") technology, including a first voltage regulator that provides a supply voltage to the circuit section at a voltage and current level suitable for use by the processor's information processing features ("cores") during operating mode, as explained more fully below.</p> <p><i>See, e.g.:</i></p>

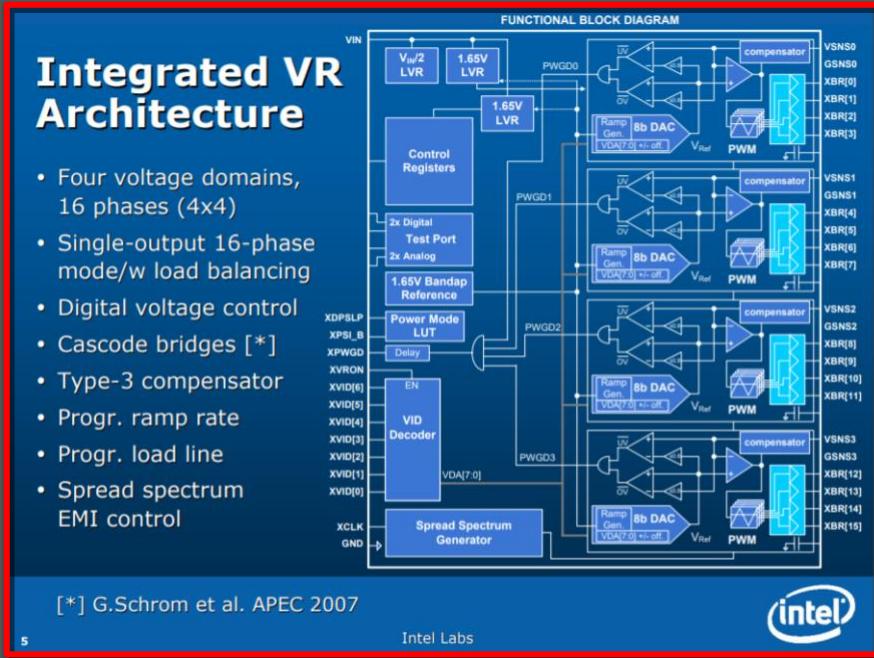
Claim 1	Accused Products
	<p><b>12.1.2 Integrated Voltage Regulator</b></p> <p>Due to the integration of platform voltage regulators into the processor, the processor has one main voltage rail (<math>V_{CCIN}</math>), the PCH has one main voltage rail (<math>V_{CCIN\_AUX}</math>) and a voltage rail for the memory interface (<math>V_{DDQ}</math>).  The voltage rail <math>V_{CCIN}</math> will supply the integrated voltage regulators which in turn will regulate to the appropriate voltages for the Cores, cache, System Agent, TCSS and graphics. This integration allows the processor to better control on-die voltages to optimize between performance and power savings. The <math>V_{CCIN}</math> rail will remain a VID-based voltage with a loadline similar to the core voltage rail in previous processors.</p> <p>Excerpt from 10th Gen Intel Core Processor Families Datasheet, Vol. 1, available at <a href="https://www.intel.com/content/dam/www/public/us/en/documents/datasheets/10th-gen-core-families-datasheet-vol-1-datasheet.pdf">https://www.intel.com/content/dam/www/public/us/en/documents/datasheets/10th-gen-core-families-datasheet-vol-1-datasheet.pdf</a></p>

Claim 1	Accused Products
	<p data-bbox="348 213 460 241">Claim 1</p> <p data-bbox="1157 213 1385 241">Accused Products</p> <div style="border: 1px solid red; padding: 10px;"> <p data-bbox="671 409 988 486"><b>Integrated VR Architecture</b></p> <ul data-bbox="671 518 958 882" style="list-style-type: none"> <li>• Four voltage domains, 16 phases (4x4)</li> <li>• Single-output 16-phase mode w/ load balancing</li> <li>• Digital voltage control</li> <li>• Cascode bridges [*]</li> <li>• Type-3 compensator</li> <li>• Progr. ramp rate</li> <li>• Progr. load line</li> <li>• Spread spectrum EMI control</li> </ul>  <p data-bbox="692 948 1009 975">[*] G.Schrom et al. APEC 2007</p> <p data-bbox="1036 980 1115 1002">5</p> <p data-bbox="1396 943 1486 997">intel</p> </div> <p data-bbox="629 1046 1776 1114">Screenshot, with annotation illustrating the plurality of voltage regulators within the Intel processor, of which one is the first voltage regulator, from</p> <p data-bbox="629 1122 1833 1192"><a href="https://www.psma.com/sites/default/files/uploads/tech-forums-packaging/presentations/is87-package-and-platform-view-intel%2080%99s-fully-integrated-coltage-regulator.pdf">https://www.psma.com/sites/default/files/uploads/tech-forums-packaging/presentations/is87-package-and-platform-view-intel%2080%99s-fully-integrated-coltage-regulator.pdf</a></p>

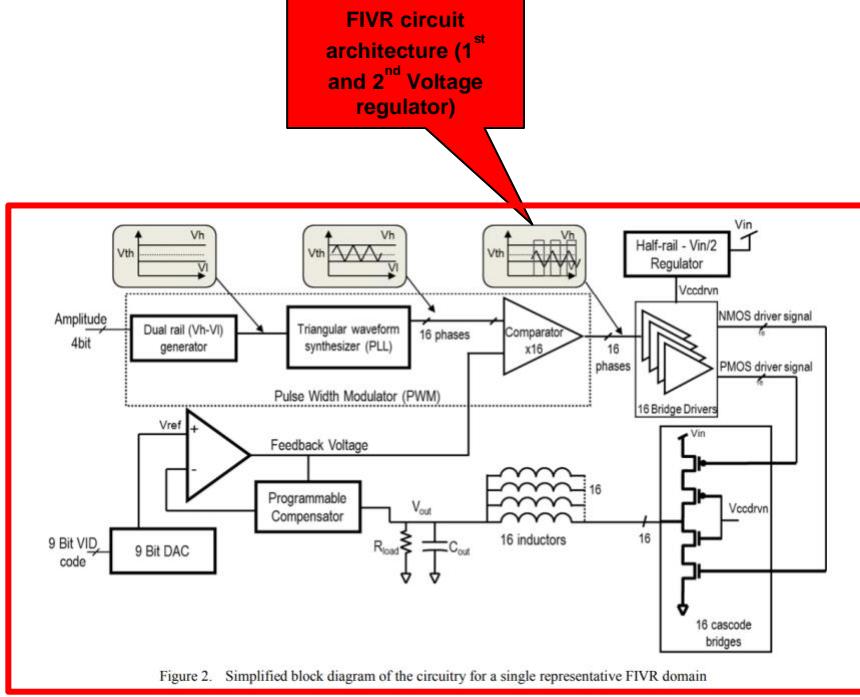
Claim 1	Accused Products
	<p><b>Haswell Platform</b></p> <p>Screenshot, with annotation, from <a href="https://www.psma.com/sites/default/files/uploads/tech-forums-packaging/presentations/is87-package-and-platform-view-intel%20%99s-fully-integrated-coltage-regulator.pdf">https://www.psma.com/sites/default/files/uploads/tech-forums-packaging/presentations/is87-package-and-platform-view-intel%20%99s-fully-integrated-coltage-regulator.pdf</a></p>

Claim 1	Accused Products
	<p style="text-align: center;"><b>FIVR circuit architecture (1<sup>st</sup> and 2<sup>nd</sup> Voltage regulator)</b></p>  <p>Figure 2. Simplified block diagram of the circuitry for a single representative FIVR domain</p> <p>Screenshot, with annotation, from <a href="https://www.researchgate.net/publication/271416878_FIVR_-Fully_integrated_voltage_regulators_on_4th_generation_IntelR_Core_SoCs">https://www.researchgate.net/publication/271416878_FIVR_-Fully_integrated_voltage_regulators_on_4th_generation_IntelR_Core_SoCs</a></p>
[1b] a second voltage regulator; and	<p>Each Accused Product includes a second voltage regulator.</p> <p>For example, the XPS 13 7390 includes an Intel 10th-generation Core processor featuring Intel's Fully Integrated Voltage Regulator ("FIVR") technology, including a second voltage regulator that provides a standby voltage to the circuit section at a voltage and current level suitable for use by the processor's memory element ("cache") during sleep mode, as explained more fully below.</p> <p><i>See, e.g.:</i></p>

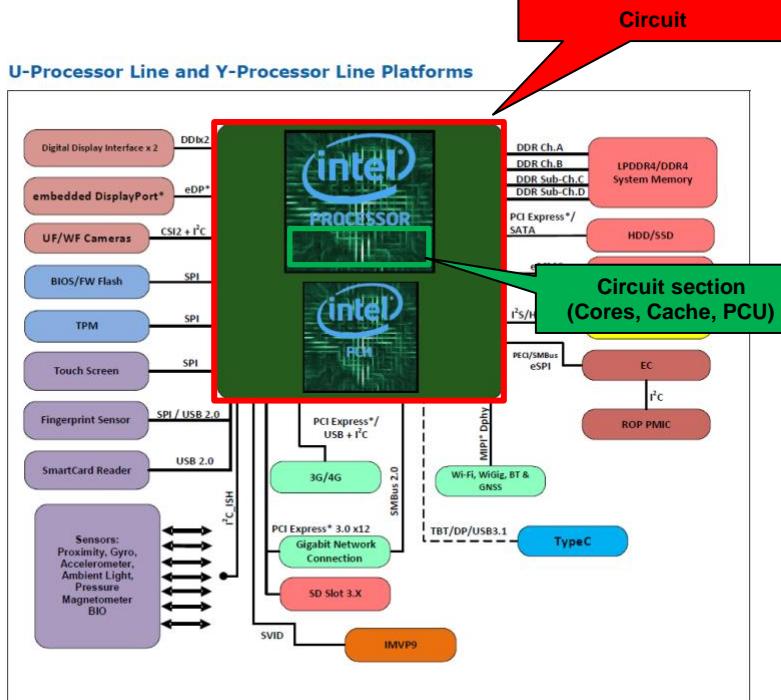
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	<p><b>12.1.2 Integrated Voltage Regulator</b></p> <p>Due to the integration of platform voltage regulators into the processor, the processor has one main voltage rail (<math>V_{CCIN}</math>), the PCH has one main voltage rail (<math>V_{CCIN\_AUX}</math>) and a voltage rail for the memory interface (<math>V_{DDQ}</math>).  The voltage rail <math>V_{CCIN}</math> will supply the integrated voltage regulators which in turn will regulate to the appropriate voltages for the Cores, cache, System Agent, TCSS and graphics. This integration allows the processor to better control on-die voltages to optimize between performance and power savings. The <math>V_{CCIN}</math> rail will remain a VID-based voltage with a loadline similar to the core voltage rail in previous processors.</p> <p>Excerpt from 10th Gen Intel Core Processor Families Datasheet, Vol. 1, available at <a href="https://www.intel.com/content/dam/www/public/us/en/documents/datasheets/10th-gen-core-families-datasheet-vol-1-datasheet.pdf">https://www.intel.com/content/dam/www/public/us/en/documents/datasheets/10th-gen-core-families-datasheet-vol-1-datasheet.pdf</a></p>

Claim 1	Accused Products
	<p data-bbox="348 218 460 246">Claim 1</p>  <p data-bbox="1558 274 1755 318"><b>Plurality of voltage regulators (FIVR)</b></p> <p data-bbox="671 409 988 491"><b>Integrated VR Architecture</b></p> <ul data-bbox="671 518 958 882" style="list-style-type: none"> <li>• Four voltage domains, 16 phases (4x4)</li> <li>• Single-output 16-phase mode w/ load balancing</li> <li>• Digital voltage control</li> <li>• Cascode bridges [*]</li> <li>• Type-3 compensator</li> <li>• Progr. ramp rate</li> <li>• Progr. load line</li> <li>• Spread spectrum EMI control</li> </ul> <p data-bbox="692 948 1009 975">[*] G.Schrom et al. APEC 2007</p> <p data-bbox="1036 980 1121 1002">5</p> <p data-bbox="1396 943 1495 997">intel</p> <p data-bbox="642 1046 1833 1192">Screenshot, with annotation illustrating the plurality of voltage regulators within the Intel processor, of which one is the second voltage regulator, from  <a href="https://www.psma.com/sites/default/files/uploads/tech-forums-packaging/presentations/is87-package-and-platform-view-intel%2080%99s-fully-integrated-coltage-regulator.pdf">https://www.psma.com/sites/default/files/uploads/tech-forums-packaging/presentations/is87-package-and-platform-view-intel%2080%99s-fully-integrated-coltage-regulator.pdf</a></p>

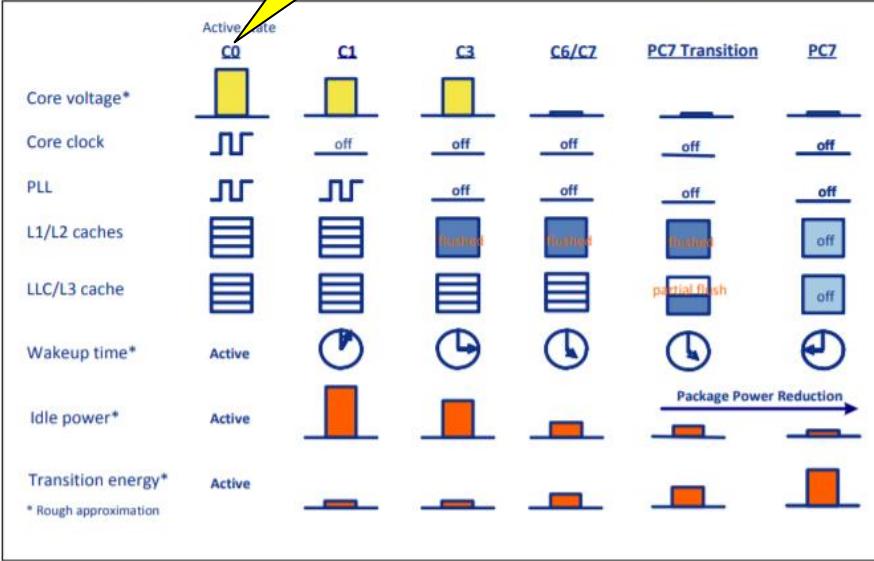
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	<p><b>Haswell Platform</b></p> <p>Screenshot, with annotation, from <a href="https://www.psma.com/sites/default/files/uploads/tech-forums-packaging/presentations/is87-package-and-platform-view-intel%20%99s-fully-integrated-voltage-regulator.pdf">https://www.psma.com/sites/default/files/uploads/tech-forums-packaging/presentations/is87-package-and-platform-view-intel%20%99s-fully-integrated-voltage-regulator.pdf</a></p>

Claim 1	Accused Products
	<p style="text-align: center;"><b>FIVR circuit architecture (1<sup>st</sup> and 2<sup>nd</sup> Voltage regulator)</b></p>  <p>Figure 2. Simplified block diagram of the circuitry for a single representative FIVR domain</p>
<p>[1c] a circuit section, the circuit section comprising a memory element and operable to:</p> <p><i>See, e.g.:</i></p>	<p>Each Accused Product includes a circuit section, the circuit section comprising a memory element. For example, the XPS 13 7390 includes an Intel 10th-generation Core processor featuring a Last Level Cache (“LLC”). The claimed circuit section comprises the LLC, the processor’s information processing unit (cores), and the power control unit.</p>

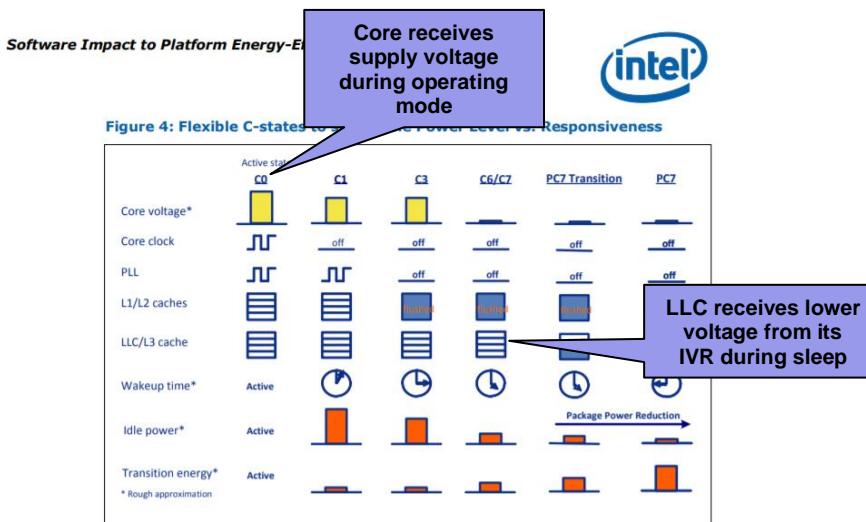
Claim 1	Accused Products
	<p><b>2.4.1 Intel® Smart Cache Technology</b></p> <p>The Intel® Smart Cache Technology is a shared Last Level Cache (LLC).</p> <ul style="list-style-type: none"> <li>• The LLC may also be referred to as a third level cache.</li> <li>• The LLC is shared between all IA cores as well as the Processor Graphics.</li> <li>• The first and second level caches are not shared between physical cores and each physical core has a separate set of caches.</li> <li>• The size of the LLC is SKU specific with a maximum of 2 MB per physical core and is a 16 way associative cache.</li> </ul> <p>Excerpt from 10th Gen Intel Core Processor Families Datasheet, Vol. 1, available at  <a href="https://www.intel.com/content/dam/www/public/us/en/documents/datasheets/10th-gen-core-families-datasheet-vol-1-datasheet.pdf">https://www.intel.com/content/dam/www/public/us/en/documents/datasheets/10th-gen-core-families-datasheet-vol-1-datasheet.pdf</a></p>

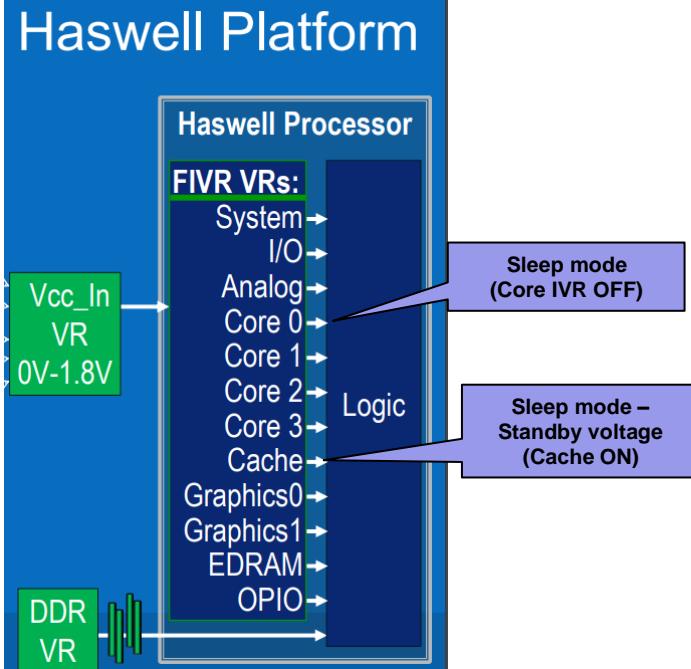
Claim 1	Accused Products
	<p style="text-align: center;"><b>Figure 1-1. U-Processor Line and Y-Processor Line Platforms</b></p>  <p>The diagram illustrates the internal architecture of Intel U-Processor and Y-Processor platforms. At the center is the <b>Circuit section (Cores, Cache, PCU)</b>, highlighted by a green box. This section connects to various components via several buses:</p> <ul style="list-style-type: none"> <li><b>I<sup>2</sup>C</b>: Sensors (Proximity, Gyro, Accelerometer, Ambient Light, Pressure, Magnetometer, BIO) and a SmartCard Reader.</li> <li><b>PCI Express*/USB + I<sup>2</sup>C</b>: 3G/4G, Gigabit Network Connection, SD Slot 3.X.</li> <li><b>SMBus 2.0</b>: Wi-Fi, WiGig, BT &amp; GNSS.</li> <li><b>PCI Express* 3.0 x12</b>: TBT/DP/USB3.1, TypeC.</li> <li><b>DDR Ch.A, DDR Ch.B, DDR Sub-Ch.C, DDR Sub-Ch.D</b>: LPDDR4/DDR4 System Memory.</li> <li><b>PCI Express*/SATA</b>: HDD/SSD.</li> <li><b>PCH</b>: EC, ROP PMIC.</li> <li><b>IMVP9</b>: SVID.</li> </ul> <p>A red arrow points from the top right to the <b>Circuit</b> area, which is labeled with a red box.</p> <p>Annotated screenshot showing circuit and circuit section from <a href="https://www.intel.com/content/www/us/en/products/docs/processors/core/10th-gen-core-families-datasheet-vol-1.html">https://www.intel.com/content/www/us/en/products/docs/processors/core/10th-gen-core-families-datasheet-vol-1.html</a>.</p>
<p>[1d] receive a supply voltage from the first voltage regulator when in an operating mode;</p> <p><i>See, e.g.:</i></p>	<p>In each Accused Product, the circuit section is operable to receive a supply voltage from the first voltage regulator when in an operating mode.</p> <p>For example, the XPS 13 7390 receives a certain core voltage from the first voltage regulator while in an operating mode, such as a C0 state (“The normal operating state of a processor IA core where code is being executed”).</p>

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	<p style="text-align: center;"><b>operating mode</b></p> <p><b>Table 3-4. Core C-states</b></p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th data-bbox="762 360 952 425">Core C-State</th><th data-bbox="952 360 1058 425">C-State Request Instruction</th><th data-bbox="1058 360 1501 425">Description</th></tr> </thead> <tbody> <tr> <td data-bbox="762 425 952 458"><b>C0</b></td><td data-bbox="952 425 1058 458">N/A</td><td data-bbox="1058 425 1501 458">The normal operating state of a processor IA core where code is being executed</td></tr> </tbody> </table> <p>Excerpt from 10th Gen Intel Core Processor Families Datasheet, Vol. 1, available at <a href="https://www.intel.com/content/dam/www/public/us/en/documents/datasheets/10th-gen-core-families-datasheet-vol-1-datasheet.pdf">https://www.intel.com/content/dam/www/public/us/en/documents/datasheets/10th-gen-core-families-datasheet-vol-1-datasheet.pdf</a></p>	Core C-State	C-State Request Instruction	Description	<b>C0</b>	N/A	The normal operating state of a processor IA core where code is being executed
Core C-State	C-State Request Instruction	Description					
<b>C0</b>	N/A	The normal operating state of a processor IA core where code is being executed					

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	<p><b>Software Impact to Platform Energy</b></p> <p style="text-align: center;"><b>Operating mode (first voltage regulator on)</b></p>  <p><b>Figure 4: Flexible C-state select Idle Power Level vs. Responsiveness</b></p>  <p>The diagram illustrates the power state selection for different components based on responsiveness. Components include Core voltage*, Core clock, PLL, L1/L2 caches, LLC/L3 cache, Wakeup time*, Idle power*, and Transition energy*. The columns represent operating modes: Active, C0, C1, C3, C6/C7, PC7 Transition, and PC7. The diagram shows how each component's power consumption and behavior change as it transitions between these modes.</p> <p>Annotated screenshot from <a href="https://www.intel.ru/content/dam/doc/white-paper/energy-efficient-platforms-2011-white-paper.pdf">https://www.intel.ru/content/dam/doc/white-paper/energy-efficient-platforms-2011-white-paper.pdf</a></p>
<p>[1e] transition from the operating mode to a sleep mode, the transition comprising deactivation of inputs of the circuit section; and</p>	<p>In each Accused Product, the circuit section is operable to transition from the operating mode to a sleep mode, the transition comprising deactivation of inputs of the circuit section.</p> <p>For example, the Intel processor in the XPS 13 7390 can transition into a sleep mode, such as the C6 state, in which the information processor units flush their L1 instruction/data caches and L2 caches, save their architectural state, deactivate their inputs, and deactivate the first voltage regulator.</p>

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	<p>See, e.g.:</p> <p><b>Table 3-4. Core C-states</b></p> <table border="1" data-bbox="840 355 1600 595"> <thead> <tr> <th data-bbox="846 360 967 381">Core C-State</th> <th data-bbox="967 360 1087 381">C-State Request Instruction</th> <th data-bbox="1087 360 1600 381">Description</th> </tr> </thead> <tbody> <tr> <td data-bbox="846 393 967 414">C0</td> <td data-bbox="967 393 1087 414">N/A</td> <td data-bbox="1087 393 1600 414">The normal state executed</td> </tr> <tr> <td data-bbox="846 425 967 447">C1</td> <td data-bbox="967 425 1087 447">MWAIT(C1)</td> <td data-bbox="1087 425 1600 470">AutoHalt - Core execution stopped, during which the package is being cooled (package in C0 state)</td> </tr> <tr> <td data-bbox="846 481 967 502">C1E</td> <td data-bbox="967 481 1087 502">MWAIT(C1E)</td> <td data-bbox="1087 481 1600 509">Core C1 + lowest frequency and voltage operating point (package in C0 state)</td> </tr> <tr> <td data-bbox="846 530 967 551">C6-C10</td> <td data-bbox="967 530 1087 595">MWAIT(C6/7/8/C8/9/10) or IO read=p_LVL3/4/5/6/7/8</td> <td data-bbox="1087 530 1600 595">Processor IA, flush their L1 instruction cache, L1 data cache, and L2 cache to the LLC shared cache cores save their architectural state to a SRAM before reducing IA cores voltage, if possible may also be reduced to 0V. Core clocks are off.</td> </tr> </tbody> </table> <p>Excerpt from 10th Gen Intel Core Processor Families Datasheet, Vol. 1, available at <a href="https://www.intel.com/content/dam/www/public/us/en/documents/datasheets/10th-gen-core-families-datasheet-vol-1-datasheet.pdf">https://www.intel.com/content/dam/www/public/us/en/documents/datasheets/10th-gen-core-families-datasheet-vol-1-datasheet.pdf</a></p> <p><b>Software Impact to Platform Energy</b></p> <p><b>Sleep mode (Core IVR off)</b></p> <p><b>Figure 4: Flexible C-states to select Idle Power Level vs. Responsiveness</b></p> <table border="1" data-bbox="756 861 1353 1241"> <thead> <tr> <th></th> <th>C0</th> <th>C1</th> <th>C3</th> <th>C6/C7</th> <th>PC7 Transition</th> <th>PC7</th> </tr> </thead> <tbody> <tr> <td>Core voltage*</td> <td>High</td> <td>Medium</td> <td>Medium</td> <td>Low</td> <td>Low</td> <td>Low</td> </tr> <tr> <td>Core clock</td> <td>On</td> <td>Off</td> <td>Off</td> <td>Off</td> <td>Off</td> <td>Off</td> </tr> <tr> <td>PLL</td> <td>On</td> <td>On</td> <td>Off</td> <td>Off</td> <td>Off</td> <td>Off</td> </tr> <tr> <td>L1/L2 caches</td> <td>On</td> <td>On</td> <td>Off</td> <td>Off</td> <td>Off</td> <td>Off</td> </tr> <tr> <td>LLC/L3 cache</td> <td>On</td> <td>On</td> <td>On</td> <td>On</td> <td>Partial Flush</td> <td>Off</td> </tr> <tr> <td>Wakeup time*</td> <td>Active</td> <td>Slow</td> <td>Slow</td> <td>Slow</td> <td>Slow</td> <td>Fast</td> </tr> <tr> <td>Idle power*</td> <td>High</td> <td>Medium</td> <td>Low</td> <td>Low</td> <td colspan="2">Package Power Reduction</td> </tr> <tr> <td>Transition energy*</td> <td>High</td> <td>Medium</td> <td>Medium</td> <td>Medium</td> <td>Medium</td> <td>Low</td> </tr> </tbody> </table> <p>* Rough approximation</p> <p>Illustrated screenshot from <a href="https://www.intel.ru/content/dam/doc/white-paper/energy-efficient-platforms-2011-white-paper.pdf">https://www.intel.ru/content/dam/doc/white-paper/energy-efficient-platforms-2011-white-paper.pdf</a></p>	Core C-State	C-State Request Instruction	Description	C0	N/A	The normal state executed	C1	MWAIT(C1)	AutoHalt - Core execution stopped, during which the package is being cooled (package in C0 state)	C1E	MWAIT(C1E)	Core C1 + lowest frequency and voltage operating point (package in C0 state)	C6-C10	MWAIT(C6/7/8/C8/9/10) or IO read=p_LVL3/4/5/6/7/8	Processor IA, flush their L1 instruction cache, L1 data cache, and L2 cache to the LLC shared cache cores save their architectural state to a SRAM before reducing IA cores voltage, if possible may also be reduced to 0V. Core clocks are off.		C0	C1	C3	C6/C7	PC7 Transition	PC7	Core voltage*	High	Medium	Medium	Low	Low	Low	Core clock	On	Off	Off	Off	Off	Off	PLL	On	On	Off	Off	Off	Off	L1/L2 caches	On	On	Off	Off	Off	Off	LLC/L3 cache	On	On	On	On	Partial Flush	Off	Wakeup time*	Active	Slow	Slow	Slow	Slow	Fast	Idle power*	High	Medium	Low	Low	Package Power Reduction		Transition energy*	High	Medium	Medium	Medium	Medium	Low
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C6-C10	MWAIT(C6/7/8/C8/9/10) or IO read=p_LVL3/4/5/6/7/8	Processor IA, flush their L1 instruction cache, L1 data cache, and L2 cache to the LLC shared cache cores save their architectural state to a SRAM before reducing IA cores voltage, if possible may also be reduced to 0V. Core clocks are off.																																																																													
	C0	C1	C3	C6/C7	PC7 Transition	PC7																																																																									
Core voltage*	High	Medium	Medium	Low	Low	Low																																																																									
Core clock	On	Off	Off	Off	Off	Off																																																																									
PLL	On	On	Off	Off	Off	Off																																																																									
L1/L2 caches	On	On	Off	Off	Off	Off																																																																									
LLC/L3 cache	On	On	On	On	Partial Flush	Off																																																																									
Wakeup time*	Active	Slow	Slow	Slow	Slow	Fast																																																																									
Idle power*	High	Medium	Low	Low	Package Power Reduction																																																																										
Transition energy*	High	Medium	Medium	Medium	Medium	Low																																																																									

Claim 1	Accused Products
<p>[1f] receive a standby voltage from the second voltage regulator when in the sleep mode, the standby voltage being less than the supply voltage and sufficient to preserve an information item stored in the memory element.</p> <p><i>See, e.g.</i></p>	<p>In each Accused Product, the circuit section is operable to receive a standby voltage from the second voltage regulator when in the sleep mode, the standby voltage being less than the supply voltage and sufficient to preserve an information item stored in the memory element.</p> <p>For example, the Intel processor in the XPS 13 7390 continues to operate the integrated voltage regulator associated with the Last Level Cache during sleep mode (such as the C6 core state) in order to receive a lower voltage sufficient to preserve the contents of the LLC memory.</p>  <p>The diagram illustrates the relationship between system power levels and responsiveness for various components across different C-state transitions. Components include Core voltage, Core clock, PLL, L1/L2 caches, LLC/L3 cache, Wakeup time, Idle power, and Transition energy. The Y-axis shows Active, C0, C1, C3, C6/C7, PC7 Transition, and PC7. The X-axis shows Off, Reduced, and Active. Annotations highlight that the Core receives supply voltage during operating mode and the LLC receives lower voltage from its IVR during sleep.</p> <p>Illustrated screenshot from <a href="https://www.intel.ru/content/dam/doc/white-paper/energy-efficient-platforms-2011-white-paper.pdf">https://www.intel.ru/content/dam/doc/white-paper/energy-efficient-platforms-2011-white-paper.pdf</a></p>

Claim 1	Accused Products
	<p style="text-align: center;"><b>Haswell Platform</b></p>  <p>Illustrated screenshot from <a href="https://www.psma.com/sites/default/files/uploads/tech-forums-packaging/presentations/is87-package-and-platform-view-intel%20%99s-fully-integrated-voltage-regulator.pdf">https://www.psma.com/sites/default/files/uploads/tech-forums-packaging/presentations/is87-package-and-platform-view-intel%20%99s-fully-integrated-voltage-regulator.pdf</a></p>

### Claim 10

Claim 10	Accused Products
[10pre] A method comprising:	To the extent the preamble is limiting, each Accused Product performs the claimed method. <i>See supra</i> claim element [1pre].
[10a] delivering to a circuit section of a circuit a supply voltage from a first voltage	Each Accused Product performs delivering to a circuit section of a circuit a supply voltage from a first voltage regulator when in an operating mode.

Claim 10	Accused Products
regulator when in an operating mode;	<i>See supra</i> claim element [1d].
[10b] transitioning from the operating mode to a sleep mode, the transition comprising deactivation of inputs of the circuit section; and	Each Accused Product performs transitioning from the operating mode to a sleep mode, the transition comprising deactivation of inputs of the circuit section. <i>See supra</i> claim element [1e].
[10c] delivering to the circuit section a standby voltage from a second voltage regulator when in the sleep mode, the standby voltage being less than the supply voltage and sufficient to preserve an information item stored in a memory element.	Each Accused Product performs delivering to the circuit section a standby voltage from a second voltage regulator when in the sleep mode, the standby voltage being less than the supply voltage and sufficient to preserve an information item stored in a memory element. <i>See supra</i> claim element [1f].